Claims

What is claimed is:

1. A method for forming a semiconductor device, comprising:

forming a plurality of container capacitor bottom plates within a base dielectric layer;

forming a supporting collar around each of the capacitor bottom plates, the supporting collar having a plurality of openings therein which expose the base dielectric layer; and

etching the base dielectric layer through the openings in the collar to expose sidewalls of the plurality of container capacitor bottom plates, wherein subsequent to etching the base dielectric layer the supporting collar supports each of the plurality of container capacitor bottom plates.

2. The method of claim 1 further comprising forming a cell dielectric on the sidewalls of the plurality of container capacitor bottom plates and on the supporting collar.

3. The method of claim 2 further comprising forming a capacitor top plate on the cell dielectric layer and over the supporting collar.

4. The method of claim 1 further comprising removing substantially all of the base dielectric layer during the etching of the base dielectric layer through the openings in the collar such that the collar contacts the plurality capacitor bottom plates and is generally free from contact with any other layer.

5. The method of claim 1 further comprising:

forming a blanket layer from a material selected from the group consisting of silicon dioxide, borophosphosilicate glass, and tetraethyl orthosilicate on a horizontal surface of the base dielectric layer; and

etching the blanket layer to form the supporting collar.

6. The method of claim 1 further comprising:

forming a blanket supporting collar layer prior to forming the container capacitor bottom plates;

etching the base dielectric layer and the blanket collar layer to form a plurality of openings therein;

forming one of the plurality of container capacitor bottom plates within each opening in the base dielectric layer and in the blanket collar layer;

only partially etching the collar layer to expose an upper sidewall of each container capacitor bottom plate; and

subsequent to only partially etching the collar layer to expose the upper sidewall of each container capacitor bottom plate, performing the etch of the base dielectric layer through the openings in the collar.

7. The method of claim 1 further comprising:

forming a blanket supporting collar layer prior to forming the container capacitor bottom plates;

forming a blanket sacrificial layer on the blanket collar layer;

etching the blanket sacrificial layer, the blanket collar layer, and the base dielectric layer to form a plurality of openings therein;

forming one of the plurality of container capacitor bottom plates within each opening in the blanket sacrificial layer, in the blanket collar layer, and in the base dielectric layer;

etching the sacrificial layer to expose an upper sidewall of each container capacitor bottom plate and to expose the collar layer; and

subsequent to etching the sacrificial layer, performing the etch of the base dielectric layer through the openings in the collar.

8. The method of claim 1 further comprising:

prior to forming the plurality of container capacitor bottom plates within the base dielectric layer, etching the base dielectric layer to form a plurality of openings therein which define container capacitor bottom plates, and a plurality of openings therein which define a plurality of moats, with one moat around each array of a semiconductor die;

forming a container capacitor bottom plate layer in the plurality of openings which define container capacitor bottom plates and in the openings which define the plurality of moats; and

during the etch of the base dielectric layer through the openings in the collar, using the container capacitor bottom plate layer in the openings which define the plurality of moats as an etch stop to protect a periphery of the semiconductor die.

9. A method used to form a semiconductor device, comprising:

forming a patterned base dielectric layer over a semiconductor wafer substrate assembly;

forming a support layer over the patterned base dielectric layer;

forming a sacrificial layer over the support layer;

removing a portion of the sacrificial layer, the support layer, and the patterned base dielectric layer to form a recess defined by the sacrificial layer, the support layer, and the patterned base dielectric layer;

forming a capacitor bottom plate within the recess, the bottom plate contacting the sacrificial layer, the support layer, and the patterned base dielectric layer;

subsequent to forming the capacitor bottom plate, removing the sacrificial layer to leave a portion of the bottom plate protruding from the support layer;

forming masking spacers along the protruding portion of the bottom plate;

etching the support layer using the masking spacers as a mask to form openings in the support layer; and

etching the base dielectric layer through the openings in the support layer,

wherein at least a portion of the support layer remains subsequent to the etching of the base dielectric layer through the openings in the support layer.

10. The method of claim 9 further comprising:

forming at least first, second, and third capacitor bottom plates such that, in cross section, a first distance between the first and second capacitor bottom plates is greater than a second distance between the second and third capacitor bottom plates;

removing the sacrificial layer to leave a portion of the first, second, and third bottom plates protruding from the support layer;

forming a masking spacer layer between the first and second capacitor bottom plate and between the second and third capacitor bottom plate such that the masking spacer layer bridges between the first and second capacitor bottom plates and bridges between the second and third capacitor bottom plates; and

performing an anisotropic etch on the masking spacer layer to form the masking spacers along the protruding portions of the bottom plates, such that, subsequent to the anisotropic etch, the masking spacer layer, in the cross section, does not bridge between first and second capacitor bottom plates and bridges between the second and third capacitor bottom plates.

11. The method of claim 9 further comprising forming the capacitor bottom plate conformal with the recess defined by the sacrificial layer, the support layer, and the patterned base dielectric layer such that the capacitor bottom plate has a recess therein.

12. The method of claim 9 further comprising:

forming a capacitor bottom plate layer to completely fill the recess defined by the sacrificial layer, the support layer, and the patterned base dielectric layer and to overlie a horizontal surface of the sacrificial layer; and

planarizing the capacitor bottom plate and the sacrificial layer to remove the capacitor bottom plate layer from the horizontal surface of the sacrificial layer and to form the capacitor bottom plate.

13. An in-process semiconductor device, comprising:

a plurality of container capacitor bottom plates, with each plate comprising a bottom and first and second cross-sectional, vertically-oriented sides each having a height, with each side being unsupported along a majority of its height;

a supporting layer having a bottom surface and a top surface, wherein the supporting layer contacts each container capacitor bottom plate of the plurality of bottom plates, and wherein the top and bottom surfaces of the supporting layer is generally free from contact with any other layer.

14. The in-process semiconductor device of claim 13, wherein the supporting layer is a material selected from the group consisting of silicon dioxide, borophosphosilicate glass, and tetraethyl orthosilicate.

15. The in-process semiconductor device of claim 13 wherein the plurality of container capacitor bottom plates comprises first, second, and third container capacitor bottom plates and the in-process semiconductor device further comprises:

the first and second capacitor bottom plates, in cross section, being spaced by a first distance;

the second and third capacitor bottom plates, in cross section, being spaced by a second distance which is less than the first distance; and

the supporting layer, in cross section, bridging between the second and third capacitor bottom plates and not bridging between the first and second capacitor bottom plates.

16. The in-process semiconductor device of claim 13 further comprising:

an array area comprising the plurality of container capacitor bottom plates and a periphery area; and

a moat between the periphery area and the array area and having a first side which faces the periphery area and a second side which faces the array area, wherein the second side is exposed and the first side is not exposed.

17. A semiconductor device comprising:

an upwardly extending container-shaped bottom electrode, wherein the bottom electrode has an interior surface, an exterior surface, a top region and a bottom region;

a lateral support structure horizontally extending from a top region of the exterior surface of the bottom electrode;

a dielectric layer covering a substantial area of the interior and exterior surfaces; and

a top electrode over at least a portion of the dielectric layer to allow capacitive coupling between the top electrode and a substantial area of both the interior and exterior surfaces.

18. The semiconductor device of claim 17 wherein the lateral support structure comprises silicon nitride.

19. The semiconductor device of claim 17 wherein the lateral support structure comprises an annular ring around the bottom electrode.

20. The semiconductor device of claim 19 wherein the bottom electrode is a first bottom electrode and the semiconductor device further comprises the annular ring lateral support structure being physically coupled to a second upwardly extending container-shaped bottom electrode laterally spaced from the first bottom electrode.

21. A pair of capacitor memory cells comprising:

first and second upwardly extending vertically-oriented bottom electrodes, wherein the bottom electrodes each have an exterior surface, a top region and a bottom region, and the first and second bottom electrodes are laterally spaced apart;

a lateral support structure horizontally extending from a top region of the exterior surface of the first bottom electrode to the top region of the exterior surface of the second bottom electrode;

a dielectric layer covering a majority of the exterior surfaces of the first and second bottom electrodes; and

a common top electrode over at least a portion of the dielectric layer to allow capacitive coupling between the top electrode and a majority of both the exterior surfaces of the first and second bottom electrodes.

22. The pair of capacitor memory cells of claim 21 wherein:

the first and second bottom electrodes each define a container having an interior surface;

the dielectric layer covers a majority of the interior surfaces of the first and second bottom electrodes; and

the top electrode over at least a portion of the dielectric layer allows capacitive coupling between the top electrode and a majority of both the interior surfaces of the first and second bottom electrodes.